

What is claimed is:

1. A method of manufacturing a semiconductor device on a semiconductor substrate, comprising:

5 forming a gate dielectric on the semiconductor substrate;
forming a gate stack overlying the gate dielectric, the gate stack having a sidewall, wherein the gate stack comprises a conductive layer and a capping nitride layer overlying the conductive layer;
selectively depositing a liner over the gate stack such that the liner is deposited on
10 the capping nitride layer at a rate lower than the rate of deposition on the conductive layer, so that the liner is thinner on the capping nitride layer than on the conductive layer; and
forming a nitride spacer over the liner.

2. The method of claim 1, wherein said forming a nitride spacer comprises:
forming a layer of nitride spacer material conformally over the liner; and
etching back the layer of nitride spacer material.

3. The method of claim 1, wherein the liner is deposited on the capping nitride layer at a rate approximately one-fifth the rate of deposition on the conductive layer.

4. The method of claim 1, wherein the liner is deposited selectively on the conductive layer in a thickness at least twice a thickness of deposition of the capping layer.

5. The method of claim 1, wherein said liner is formed of oxide.

6. A method of manufacturing a semiconductor device on a semiconductor substrate, comprising:

forming at least two adjacent gate stacks over the substrate, the adjacent gate stacks each having a sidewall opposing each other,

wherein each of the gate stacks comprises a conductive layer and a capping nitride layer overlying the conductive layer;

selectively depositing a liner over the gate stacks, so that the liner is thicker on the conductive layer than on the capping nitride layer; and

forming adjacent at least two nitride spacers on the liner, overlying the opposing sidewalls.

7. The method of claim 6, wherein the liner is deposited over the capping nitride layer at a rate lower than the rate of deposition on the conductive layer.

8. The method of claim 6, wherein said forming adjacent nitride spacers comprises:

forming a layer of nitride spacer material conformally over the liner; and etching back the layer of nitride spacer material.

9. The method of claim 6, wherein the adjacent nitride spacers have top, middle, and bottom spaces therebetween, and wherein the bottom space is substantially shorter than the middle space.

10. The method of claim 6, wherein the liner is formed of oxide.

11. The method of claim 6, further comprising a pre-metal dielectric layer overlying the gate stacks, capping layer and nitride spacers.

12. A gate structure, comprising:
a gate dielectric on a semiconductor substrate;
a gate stack overlying the gate dielectric, the gate stack having a sidewall, wherein the gate stack comprises a conductive layer and a capping nitride layer overlying the conductive layer;
an oxide liner disposed on the sidewall of the gate stack, wherein the thickness of the liner is substantially thicker on the conductive layer than on the capping nitride layer;
a nitride sidewall spacer disposed over the liner and sloped away from the gate stack adjacent the gate dielectric.

13. The gate structure of claim 12, further comprising:
a PMD layer overlying the gate stack, the nitride spacer, and the capping layer.

14. The gate structure of claim 13, further comprising:
a contact plug formed within the PMD layer adjacent the gate stack.

5
15. A gate structure, comprising:
a gate stack having a sidewall including a conductive layer;
a capping nitride layer on the conductive layer;
a liner disposed on the sidewall of the gate stack,
wherein the thickness of the liner is substantially thinner on the capping nitride layer
than on the conductive layer;
a nitride spacer formed along opposite sides of the gate stack overlying the liner, the
thickness of the nitride layer having a transition adjacent a boundary between the
15 conductive layer and the capping nitride layer.

16. A semiconductor device, comprising:
at least two adjacent gate stacks over a semiconductor substrate, the
adjacent gate stacks each having a sidewall opposing each other, wherein each of the gate
20 stack comprises a conductive layer and a capping nitride layer overlying the conductive layer;
a liner selectively deposited overlying opposing sidewalls of the gate stacks, the
liner being thinner on the capping nitride layer than on the conductive layer;
at least two adjacent nitride sidewall spacers on the liner each overlying the
opposing sidewalls.

25
17. The device of claim 16, wherein the at least two adjacent sidewall spacers
have a bottom, middle, and top space therebetween, and wherein the bottom space 36 is
substantially shorter than the middle space.

30
18. The device of claim 16, wherein the top space is wider than the middle
space.

Sub 7⁵
A1

of claim 16, wherein the
em, and the gate stacks, li
the PMD layer filling the
of claim 16, wherein the p

[illegible]